AMENDMENTS

In the Claims:

Please amend the claims according to the following listing of claims and substitute it for all prior versions and listings of claims in the application.

1. (currently amended) A hybrid integrated circuit (IC) package substrate, ~~at least~~ comprising:

a plurality of patterned conductive layers stacked over each other, wherein the outermost patterned conductive layer furthermore has a plurality of bonding pads thereon;

a plurality of dielectric layers respectively sandwiched between a pair of neighboring patterned conductive layers, wherein at least one of the dielectric ~~layer~~ layers is a ceramic dielectric layer with one ceramic dielectric layer as a dielectric core layer and at least one of the remaining dielectric layers is an organic dielectric layer, and wherein the dielectric layers are formed via a built-up method; and

a plurality of vias respectively passing through at least ~~one of~~ the dielectric core layer for connecting at least two of the patterned conductive layers electrically.

Claim 2. (canceled)

3. (currently amended) The hybrid IC package substrate of claim ~~2~~ 1, wherein the dielectric layers are symmetrically distributed on each side of the dielectric core layer.

4. (currently amended) The hybrid IC package substrate of claim ~~2~~ 1, wherein the dielectric layers are non-symmetrically distributed on each side of the dielectric core layer.

5. (currently amended) ~~The~~ A hybrid IC package substrate ~~of claim 1, wherein all the remaining dielectric layers are positioned on one side of the ceramic dielectric layer.~~, comprising:

a plurality of patterned conductive layers stacked over each other, wherein the outermost patterned conductive layer furthermore has a plurality of bonding pads thereon;

a plurality of dielectric layers respectively sandwiched between a pair of neighboring patterned conductive layers, wherein at least one of the dielectric layers is a ceramic dielectric layer with one ceramic dielectric layer positioned with all the remaining dielectric layers on one side thereof and used to be attached to the IC, and at least one of the remaining dielectric layers is an organic dielectric layer, and wherein the dielectric layers are formed via a built-up method; and

a plurality of vias respectively passing through at least the dielectric core layer for connecting at least two of the patterned conductive layers electrically.

6. (currently amended) A chip package structure, at least comprising:

a hybrid integrated circuit (IC) carrier having a first surface and a second surface, wherein the hybrid IC carrier at least having:

a plurality of patterned conductive layers stacked over each other, wherein the patterned conductive layer closest to the first surface furthermore has a plurality of bonding pads thereon;

a plurality of dielectric layers respectively sandwiched between a pair of neighboring patterned conductive layer, wherein at least one of the dielectric ~~layer~~ layers is a ceramic dielectric layer with one ceramic dielectric layer as a dielectric core layer and

at least one of the remaining dielectric layers is an organic dielectric layer, and wherein the dielectric layers are formed via a built-up method; and

a plurality of vias passing through at least ~~one of~~ the dielectric core layer for connecting at least two of the patterned conductive layers electrically; and

a chip attached to the first surface of the hybrid IC carrier and connected electrically to the hybrid IC carrier via the bonding pads.

Claim 7. (canceled)

8. (currently amended) The chip package structure of claim ~~7~~ 6, wherein the dielectric layers are symmetrically distributed on each side of the dielectric core layer.

9. (currently amended) The chip package structure of claim ~~7~~ 6, wherein the dielectric layers are non-symmetrically distributed on each side of the dielectric core layer.

10. (original) The chip package structure of claim 6, wherein all the remaining dielectric layers are positioned on one side of the ceramic dielectric layer.

11. (original) The chip package structure of claim 6, wherein the chip is electrically connected to the hybrid IC carrier through a flip chip bonding or a wire bonding process.

12. (original) The chip package structure of claim 6, wherein the package furthermore comprises a plurality of contacts attached to the second surface of the hybrid IC carrier.

13. (new) The chip package structure of claim 10, wherein the ceramic dielectric layer is attached to the chip on the first surface of the hybrid IC carrier.